WHAT IS CLAIMED IS:

1. An apparatus for decoding n reception symbols utilizing block code generator matrix information, the apparatus comprising:

a controller for determining symbol position information for relocating each of the n reception symbols utilizing the block code generator matrix information and inverse fast hadamard transform (IFHT) size information for performing an IFHT for the n reception symbols;

a symbol arranging unit for relocating each of the n reception symbols according to the symbol position information determined by the controller;

an IFHT unit for inputting the symbols relocated by the symbol arranging unit to perform the IFHT for the symbols; and

a comparator/selector for outputting, as a decoding signal, a codeword of a block code having a maximum correlation value from among result values obtained by performing the IFHT.

2. The apparatus as claimed in claim 1, wherein the block code generator matrix information represent a k×n matrix, which has k rows and n columns, for generating the block code, and the IFHT size information is information for controlling bases in k-m highly-ranked rows in the k×n matrix to be used as input of the IFHT unit.

3. The apparatus as claimed in claim 2, wherein the controller sequentially selects elements from the k×n matrix by selecting only k-m elements from a first row to an $(k-m)^{th}$ row in each of the n columns sequentially from a first column to an n^{th} column, generates binary sequences in which an element in the first row is used as a least significant bit and an element in the m-th row is used as a most significant bit, and calculates decimal numbers of each of the generated binary sequences, so that the controller determines the symbol position information in such a manner that a first reception symbol to an n^{th} reception

symbol of the reception symbols sequentially correspond to the inputs of the IFHT unit, which correspond to decimal values in the n columns from the first column to the n^{th} column, respectively.

4. The apparatus as claimed in claim 2, wherein the apparatus further comprises a mask multiplier for multiplying the n reception symbols by masks provided according to a predetermined control, and outputting the multiplication results to the symbol arranging unit.

5. The apparatus as claimed in claim 4, wherein the controller uses bases in a row-ranked m row, not including bases in a highly-ranked k-m row, in the k×n matrix as mask bases, and provides masks, which are generated by modulating the mask bases according to a modulation method applied to the block code, to the mask multiplier.

6. The apparatus as claimed in claim 3, wherein the symbol arranging unit comprises:

a switch for inputting the reception symbols, and switching respectively a first reception symbol to an n^{th} reception symbol to n adders according to the symbol position information provided by the controller;

n memories respectively connected to n inputs from a first input to an n^{th} input of the IFHT unit; and

n adders having first ends and second ends, each of the first ends being connected to the switch, and each of the second ends being connected to each of the respective n memories.

7. The apparatus as claimed in claim 6, wherein the symbol arranging unit further comprises:

n switches, each of the n switches having a first end and a second end, the first end being connected to one of the n memories, the second end being connected to the IFHT unit,

wherein the symbol arranging unit controls the n switches to be sequentially connected to the IFHT unit, sequentially from a switch connected to the first input of the IFHT unit to a switch connected to the n^{th} input of the IFHT unit, when a symbol relocation for each of the n reception symbols has been completed.

8. The apparatus as claimed in claim 6, wherein the symbol arranging unit further comprises:

a parallel-to-serial converter having a first end and a second end, the first end being connected to each of the n memories, the second end being connected to the IFHT unit,

wherein the symbol arranging unit controls the parallel-to-serial converter to perform serial conversion for signals stored in the n memories and output the converted signals to the IFHT unit, sequentially from a memory connected to the first input to a memory connected to the n^{th} input of the IFHT unit, when the symbol relocation for each of the n reception symbols has been completed.

9. An apparatus for decoding a block code including n reception symbols utilizing block code generator matrix information, the apparatus comprising:

a controller for determining inverse fast hadamard transform (IFHT) size information for performing an IFHT for the n reception symbols and symbol position information for relocating each of the n reception symbols utilizing the block code generator matrix information;

a symbol arranging unit for relocating each of the n reception symbols according to the symbol position information determined by the controller;

an IFHT unit for inputting the symbols relocated by the symbol arranging unit to perform the IFHT for the symbols; and

a comparator/selector for outputting, as a decoding signal, a codeword of the block code, which has a maximum correlation value from among result values obtained by performing the IFHT.

10. The apparatus as claimed in claim 9, wherein the block code generator matrix information represent a k×n matrix, which has k rows and n columns, for generating the block code.

11. The apparatus as claimed in claim 9, wherein the controller considers operation amount, system complexity, and IFHT implementation time when the IFHT is performed utilizing the block code generator matrix information, and uses the IFHT size information, and the IFHT size information control bases in k-m highly-ranked rows in the k×n matrix to be used as input of the IFHT unit.

12. The apparatus as claimed in claim 11, wherein the controller sequentially selects elements from the k×n matrix by selecting only m elements of the k-m highly-ranked rows from a first row to an $(k-m)^{th}$ row in each of the n columns sequentially from a first column to an n^{th} column, generates binary sequences in which an element in the first row is used as a least significant bit and an element in the m-th row is used as a most significant bit, and calculates decimal numbers of each of the generated binary sequences, so that the controller determines the symbol position information in such a manner that a first reception symbol to an n^{th} reception symbol of the reception symbols sequentially correspond to the inputs of the IFHT unit, which correspond to decimal values in the n columns from the first column to the n^{th} column, respectively.

13. The apparatus as claimed in claim 11, wherein the apparatus further comprises a mask multiplier for multiplying the reception symbols by masks provided according to a predetermined control, and for outputting the multiplication results to the symbol arranging unit.

14. The apparatus as claimed in claim 13, wherein the controller uses bases in a row-ranked m row, not including bases in a highly-ranked k-m row, in the k×n matrix as mask bases, and provides masks, which are generated by modulating the mask bases according to a modulation method applied to the block code, to the mask multiplier.

15. The apparatus as claimed in claim 12, wherein the symbol arranging unit comprises:

a switch for inputting the reception symbols, and switching respectively a first reception symbol to an n^{th} reception symbol to n adders according to the symbol position information provided by the controller;

n memories respectively connected to n inputs from a first input to an n^{th} input of the IFHT unit; and

n adders having first ends and second ends, each of the first ends being connected to the switch, and each of the second ends being connected to each of the respective n memories.

16. The apparatus as claimed in claim 15, wherein the symbol arranging unit further comprises:

n switches, each of the n switches having a first end and a second end, the first end being connected to one of the n memories, the second end being connected to the IFHT unit,

wherein the symbol arranging unit controlling the n switches to be sequentially connected to the IFHT unit, sequentially from a switch connected to the first input of the IFHT unit to a switch connected to the n^{th} input of the IFHT

unit, when a symbol relocation for each of the n reception symbols has been completed.

17. The apparatus as claimed in claim 15, wherein the symbol arranging unit further comprises:

a parallel-to-serial converter having a first end and a second end, the first end being connected to each of the n memories, the second end being connected to the IFHT unit,

wherein the symbol arranging unit controls the parallel-to-serial converter to perform serial conversion for signals stored in the n memories and output the converted signals to the IFHT unit, sequentially from a memory connected to the first input to a memory connected to the n^{th} input of the IFHT unit, when the symbol relocation for each of the n reception symbols has been completed.

18. A method for decoding n reception symbols utilizing block code generator matrix information, the method comprising the steps of:

a) determining symbol position information for relocating each of the n reception symbols utilizing the block code generator matrix information and inverse fast hadamard transform (IFHT) size information for performing an IFHT for the n reception symbols;

b) relocating each of the n reception symbols as an input of an IFHT unit according to the determined symbol position information;

c) inputting the relocated symbols to perform the IFHT for the symbols; and

d) outputting, as a decoding signal, a codeword of a block code, which has a maximum correlation value from among result values obtained by performing the IFHT.

19. The method as claimed in claim 18, wherein the block code generator matrix information represent a k×n matrix, which has k rows and n columns, for generating the block code, and the IFHT size information is information for controlling bases in k-m highly-ranked rows in the k×n matrix to be used as input of the IFHT unit.

20. The method as claimed in claim 19, wherein said step a) comprises:

selecting elements from the k×n matrix by selecting only m elements of the k-m highly-ranked rows from a first row to an $(k-m)^{th}$ row in each of the n columns sequentially from a first column to an n^{th} column in the k×n matrix;

generating binary sequences in which an element in a first row is used as a least significant bit and an element in an $(k-m)^{th}$ row is used as a most significant bit;

calculating a decimal number value of each of the generated binary sequences; and

determining the symbol position information so that a first reception symbol to an n^{th} reception symbol of the reception symbols sequentially correspond to the inputs of the IFHT, which correspond to decimal values in the n columns from the first column to the n^{th} column.

21. The method as claimed in claim 19, further comprising the steps of:

multiplying the reception symbols by masks provided according to a predetermined control; and

relocating the symbols.

22. The method as claimed in claim 21, wherein the masks are generated by modulating bases in a row-ranked m row, not including bases in a

highly-ranked (k-m) row, in the k×n matrix according to a modulation method applied to the block code.

23. A method for decoding n reception symbols utilizing block code generator matrix information, the method comprising the steps of:

a) determining inverse fast hadamard transform (IFHT) size information for performing an IFHT for the n reception symbols and symbol position information for relocating each of the n reception symbols utilizing the block code generator matrix information;

b) relocating each of the n reception symbols as an input of an IFHT unit according to the determined symbol position information;

c) inputting the relocated symbols to perform the IFHT for the symbols; and

d) outputting, as a decoding signal, a codeword of a block code, which has a maximum correlation value from among result values obtained by performing the IFHT.

24. The method as claimed in claim 23, wherein the block code generator matrix information represent a k×n matrix, which has k rows and n columns, for generating the block code.

25. The method as claimed in claim 23, wherein the IFHT size information is determined by considering operation amount, system complexity, and IFHT implementation time when the IFHT is performed utilizing the block code generator matrix information, and the IFHT size information is information for controlling bases in (k-m) highly-ranked rows in the k×n matrix to be used as the input of the IFHT unit.

26. The method as claimed in claim 25, wherein said step a) comprises the steps of:

selecting elements from the k×n matrix by selecting only m elements of the (k-m) highly-ranked rows from a first row to an $(k-m)^{th}$ row in each of the n columns sequentially from a first column to an n^{th} column in the k×n matrix;

generating binary sequences in which an element in a first row is used as a least significant bit and an element in an $(k-m)^{th}$ row is used as a most significant bit;

calculating a decimal number value of each of the generated binary sequences; and

determining the symbol position information so that a first reception symbol to an n^{th} reception symbol of the reception symbols sequentially correspond to the inputs of the IFHT, which correspond to decimal values in the n columns from the first column to the n^{th} column.

27. The method as claimed in claim 25, further comprising the steps of:

multiplying the reception symbols by masks provided according to a predetermined control; and

relocating the symbols.

28. The method as claimed in claim 27, wherein the masks are generated by modulating bases in a row-ranked m row, not including bases in a highly-ranked k-m row, in the k×n matrix according to a modulation method applied to the block code.

29. An apparatus for decoding n reception symbols utilizing a block code generator matrix having k rows and n columns, the apparatus comprising:

a controller for inputting the n reception symbols and calculating symbol positions for the n columns in the block code generator matrix; and

a symbol arranging unit including adders for accumulating and relocating the n reception symbols at the calculated symbol positions.

30. The apparatus as claimed in claim 29, wherein the apparatus further comprises:

an inverse fast hadamard transform (IFHT) unit for inputting the accumulated symbols by the symbol arranging unit and performing an IFHT for the symbols: and

a comparator/selector for decoding n bits, which have a maximum correlation value from among results obtained by performing the IFHT, as information bits.

31. The apparatus as claimed in claim 30, wherein the apparatus further comprises a mask multiplier for multiplying the n reception symbols by masks provided according to a predetermined control, and outputting the multiplication result to the symbol arranging unit.

32. The apparatus as claimed in claim 31, wherein the controller uses bases in a row-ranked m row, not including bases in a highly-ranked (k-m) row, in the block code generator matrix as mask bases, and provides masks, which are generated by modulating the mask bases according to a modulation method applied to a block code, to the mask multiplier.

33. A method for decoding n reception symbols utilizing a block code generator matrix having k rows and n columns, the method comprising the steps of:

calculating symbol positions for the n columns in the block code generator matrix; and

accumulating and relocating the n reception symbols at the calculated symbol positions.

34. The method as claimed in claim 33, further comprising the steps of:

inputting the accumulated symbols and performing an inverse fast hadamard transform (IFHT) for the symbols: and

decoding n bits, which have a maximum correlation value from among results obtained by performing the IFHT, as information bits.

35. The method as claimed in claim 34, further comprising the steps of:

multiplying the n reception symbols by masks provided according to a predetermined control; and

relocating the symbols to the calculated symbol positions.

36. The method as claimed in claim 35, wherein the masks are generated by modulating bases in a row-ranked m row, not including bases in a highly-ranked (k-m) row, in the block code generator matrix according to a modulation method applied to a block code.